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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,378	02/06/2004	Yoshiro Shimojo	248574US2S	6785

22850 7590 01/13/2005

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EXAMINER	
HA, NGUYEN T	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,378	SHIMOJO ET AL.	
	Examiner	Art Unit	
	Nguyen T Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *13-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-7 and 9-12* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0204*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I claims 1-12 in the reply filed on 11/30/2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 4-7 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. (US 6,388,281) in view of Kikuchi et al. (US 6,682,944).

Regarding claim 1, Jung et al. disclose a semiconductor device (figures 3A-3H) comprising:

- a capacitor (column 8, line 1) configured by a bottom electrode (122 & 120, column 8, line 2), a top electrode (126 & 128, column 8, lines 10-11), and a dielectric/ferroelectric film (124, column 8, line 4) disposed between the bottom electrode and the top electrode (figure 3F);
- an insulating layer (134, column 8, line 37) which surrounds the capacitor
- (figure 3H); and
- a high-dielectric/diffusion barrier layer (132) which is disposed between the dielectric (124) and the insulating layer (134), and which entirely covers side wall portions of the dielectric (figure 3H).

Jung et al. fail to disclose a dielectric constant of the high-dielectric being higher than a dielectric constant of the insulating layer.

Kikuchi et al. teach a capacitor (figure 2J) having an insulation layer (20) formed of SiO_2 (column 7, lines 37-39) formed over a protection layer (19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an insulation layer formed of Silicon oxide (SiO_2) as taught by Kikuchi in Jung et al., in order to prevent the leakage current for the capacitor.

Regarding claim 2, Jung et al. disclose the dielectric constant of the high-dielectric (TiO_2) is higher than a dielectric constant of the dielectric (PZT) configuring the capacitor (column 7, lines 19-21).

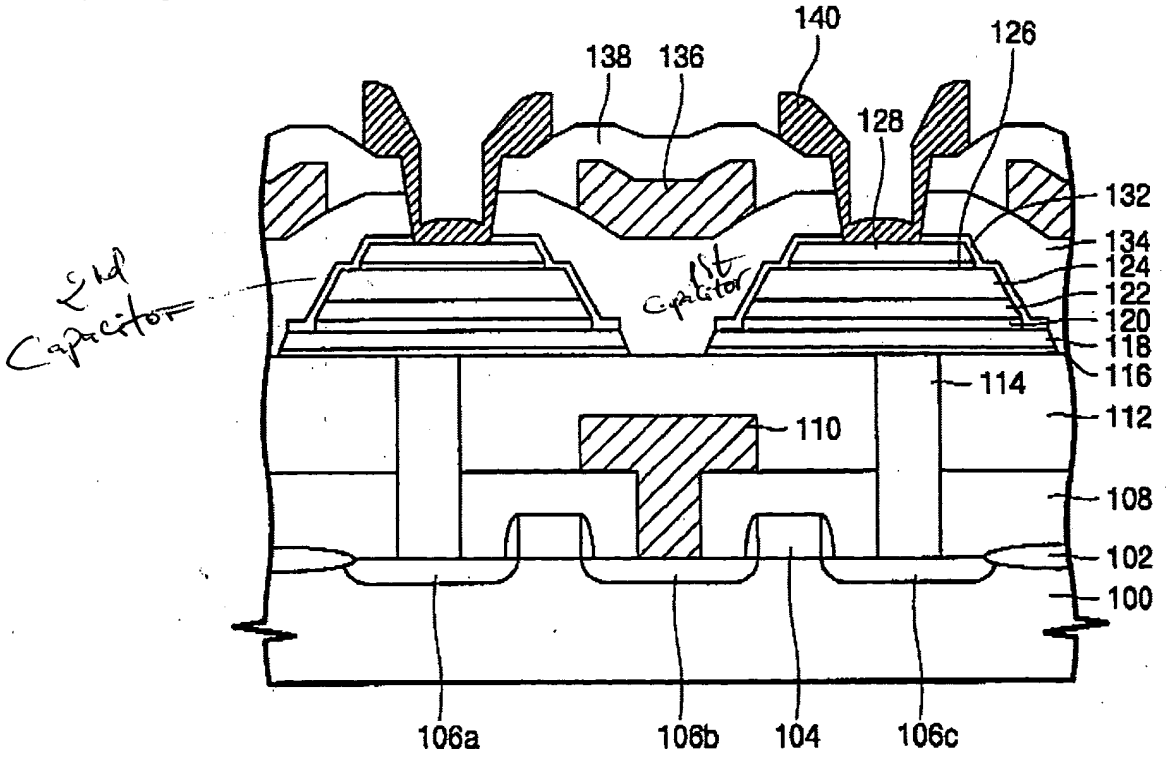
Regarding claim 4, the modified of Jung et al. show all the claimed limitations with respect to claim 1 above, Kikuchi et al. further teach the insulating layer being silicon oxide (column 7, lines 37-39).

Regarding claim 5, Jung et al. disclose the high-dielectric is configured by TiO_2 (column 8, lines 17-19).

Regarding claim 6, Jung et al. disclose the high-dielectric (132) covering the bottom electrode and the top electrode (figure 3H).

Regarding claim 7, Jung et al. further disclose the high-dielectric (132) covering only side-wall portions of the dielectric (figure 2).

Regarding claim 9, Jung et al. disclose a semiconductor device (figure 2) comprising:



- a first capacitor and a second capacitor (pointed out by examiner) each of which is configured by a bottom electrode (120 & 122, column 8, line 2), a top electrode (126 & 128, column 8, lines 10-11); and
- a dielectric/ferroelectric film (124, column 8, line 4) disposed between the bottom electrode and the top electrode (figure 2);
- an insulating layer (134, column 8, line 37) which surrounds the first capacitor and the second capacitor (figure 2); and
- a high-dielectric/diffusion barrier layer (132) which are disposed between the dielectric and the insulating layer, and which entirely covers side wall portions of the dielectric (figure 2).

Jung et al. fail to disclose a dielectric constant of the high-dielectric being higher than a dielectric constant of the insulating layer.

Kikuchi et al. teach a capacitor (figure 2J) having an insulation layer (20) formed of SiO_2 (column 7, lines 37-39) formed over a protection layer (19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an insulation layer formed of Silicon oxide (SiO_2) as taught by Kikuchi in Jung et al., in order to prevent the leakage current for the capacitor.

Regarding claim 10, Jung et al. disclose the insulating layer and the high dielectric exist at a space between the first capacitor and the second capacitor (figure 2).

Regarding claim 11, Jung et al. discloses the high-dielectric exists at a space between the first capacitor and the second capacitor (figure 2).

Regarding claim 12, Jung et al. disclose a semiconductor device (figure 2) comprising:

- a capacitor configured by a bottom electrode (120 & 122, column 8, line 2), a top electrode (126 & 128, column 8, lines 10-11), and a dielectric/ferroelectric film (124, column 8, line 4) disposed between the bottom electrode and the top electrode (figure 2);
- a transistor (104) which is connected to the bottom electrode (figure 2);
- an insulating layer (134, column 8, line 37) which surrounds the first capacitor and the second capacitor (figure 2); and
- a high-dielectric/diffusion barrier layer (132) which are disposed between the dielectric and the insulating layer, and which entirely covers side wall portions of the dielectric (figure 2).

Jung et al. fail to disclose a dielectric constant of the high-dielectric being higher than a dielectric constant of the insulating layer.

Kikuchi et al. teach a capacitor (figure 2J) having an insulation layer (20) formed of SiO_2 (column 7, lines 37-39) formed over a protection layer (19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an insulation layer formed of Silicon oxide (SiO_2) as taught by Kikuchi in Jung et al., in order to prevent the leakage current for the capacitor.

Allowable Subject Matter

4. Claims 3 & 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 3, the prior art alone or in combination does not teach the limitation of a thickness of the high-dielectric in a direction perpendicular to side surfaces of the dielectric configuring the capacitor is equal to a distance from the bottom electrode to the top electrode.

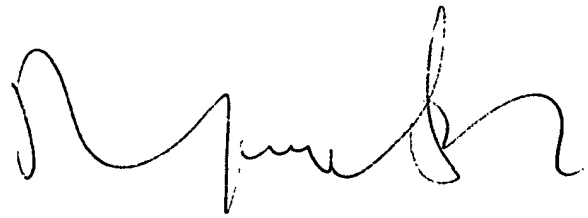
With respect to claim 8, the prior art alone or in combination does not teach the limitation of a semiconductor device comprising a barrier layer in the between of the high-dielectric and the dielectric configuring the capacitor, to prevent reaction of the high-dielectric and the dielectric is disposed.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nguyen T. Ha
January 5, 2005